6/FDS
P. Walker
9-18-01

XA-9472

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yasuhisa SHIMAZAKI et al.

Appln. No.: 09/855,660 Group Art Unit: 2811

Filed: May 16, 2001

For: SEMICONDUCTOR INTEGRATED CIRCUIT

* * *

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Pursuant to 37 C.F.R. § 1.56, and without any assertion as to materiality or prior art effect, the documents listed on the attached Form PTO-1449 are hereby cited.

The documents on the attached list are cited in the specification, on page 2, and their relevance is addressed therein.

Respectfully submitted,

By: _____
Mitchell W. Shapiro
Reg. No. 31,568

MWS:lmb

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August 6, 2001